In the Abstract:

Please cancel the Abstract of Disclosure and substitute the following:

A dual damascene process is disclosed which reduces capacitance increases caused by excess and unnecessary remnants of an etching stop layer and which also improves multi-level interconnect structures by using removing an etching stop layer except a portion that surrounds a via hole. This reduces or eliminates capacitance increase and avoids erosion of underlying interlayer insulating layers during formation of an upper, wider trench.